WHAT IS CLAIMED IS:

1. A substrate, comprising:

a non-electrically conductive core having a first side and an opposing second side,

a first electrically conductive layer disposed on the first side of the core,

a second electrically conductive layer disposed on the second side of the core,

electrically conductive core vias extending from the first side of the core to the second side of the core, the core vias disposed in an array,

an electrically conductive contact formed on an upper build-up layer on the first side of the core, the contact overlying the array of core vias,

a first electrically conductive via electrically connecting the contact to an intervening build-up layer disposed between the upper build-up layer and the first electrically conductive layer, the first via overlying the core via array, and

a second electrically conductive via electrically connecting the intervening build-up layer and the first electrically conductive layer, the second electrically conductive via not disposed over the core via array.

2. The substrate of claim 1, wherein the core via array is centrally disposed in the substrate.

3. The substrate of claim 1, wherein the core via array is too densely packed for the first electrically conductive layer to penetrate the core via array.

4. The substrate of claim 1, wherein the contact is VDDIO contact disposed in an interior portion of the substrate.

5. The substrate of claim 1, wherein the first electrically conductive layer is a VDDIO layer.

6. The substrate of claim 1, wherein the first via, intervening layer, and second via comprise a plurality of intervening layers and a plurality of electrically conductive vias electrically connecting the contact to the first electrically conductive layer.

7. The substrate of claim 1, wherein the intervening build-up layer is a signal routing layer.

8. A packaged integrated circuit including the substrate of claim 1.

9. A substrate, comprising:
a non-electrically conductive core having a first side and an opposing second side,
a first electrically conductive layer disposed on the first side of the core,
a second electrically conductive layer disposed on the second side of the core,
electrically conductive core vias extending from the first side of the core to the second side of the core, the core vias in an array centrally disposed in the substrate, wherein the core via array is too densely packed for the first electrically conductive layer to penetrate the core via array,
an electrically conductive contact formed on an upper build-up layer on the first side of the core, the contact overlying the array of core vias,
a first electrically conductive via electrically connecting the contact to an intervening signal routing layer disposed between the upper build-up layer and the first electrically conductive layer, the first via overlying the core via array, and
a second electrically conductive via electrically connecting the intervening signal routing layer and the first electrically conductive layer, the second electrically conductive via not disposed over the core via array.

10. The substrate of claim 9, wherein the contact is VDDIO contact disposed in an interior portion of the substrate.

11. The substrate of claim 9, wherein the first electrically conductive layer is a VDDIO layer.

12. The substrate of claim 9, wherein the first via, intervening layer, and second via comprise a plurality of intervening layers and a plurality of electrically conductive vias electrically connecting the contact to the first electrically conductive layer.

13. A packaged integrated circuit including the substrate of claim 9.

14. A substrate, comprising:

a non-electrically conductive core having a first side and an opposing second side,

a VDDIO layer disposed on the first side of the core,

a second electrically conductive layer disposed on the second side of the core,

four build-up layers on each of the first side and the second side of the core,

electrically conductive core vias extending from the first side of the core to the second side of the core, the core vias in an array centrally disposed in the substrate, wherein the core via array is too densely packed for the VDDIO layer to penetrate the core via array,

an electrically conductive VDDIO contact formed on an upper-most of the build-up layers on the first side of the core, the VDDIO contact overlying the centrally disposed array of core vias,

a first electrically conductive via electrically connecting the VDDIO contact to an intervening one of the build-up layers disposed between the upper-most build-up layer and the VDDIO layer, the first via overlying the core via array, where the intervening build-up layer is a signal routing layer, and

a second electrically conductive via electrically connecting the intervening signal routing layer and the VDDIO layer, the second electrically conductive via not disposed over the core via array.

15. A packaged integrated circuit including the substrate of claim 14.